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DEVICE FOR PROLONGING LIFETIME OF NONVOLATILE MEMORY

FIELD OF THE INVENTION

[0001] This invention relates generally to nonvolatile memories, and more particularly, to a device for prolonging the lifetime of a nonvolatile memory that can lessen impairment of the memory due to repeated read/write operations.

BACKGROUND OF THE INVENTION

[0002] A memory unit is defined as "nonvolatile" if no inside data is lost after disconnection of the power supply. Therefore, the nonvolatile memory plays a very important role in both the computer and the telecommunication industries.This is especially true of the flash memory, which is one of the hot products in today's nonvolatile memory market.

[0003] However, the nonvolatile flash memory is intrinsically limited with respect to operation times because the inside memory cells must be refreshed based on the principle of hot-carriers field effect, as a result of which inside data thereof must be erased and rewritten with 1s instead of previously existed 0s and 1s before writing new data. During writing, because the required operational voltage is 7V or higher, the oxidation layer in the flash memory may be impaired to some extent by repeatedly writing and erasing operations that would undoubtedly shorten its lifetime.

[0004] For improving the above said defect, only a few protective measures are available so far, such as employing arithmetic to uniformly use every block in the

flash memory and thereby potentially prolong the lifetime of the memory by as long as one million times. This known effect may be enhanced when associated with the present invention.

SUMMARY OF THE INVENTION

[0005] The primary object of this invention is to provide a device for prolonging lifetime of a nonvolatile memory such that the consumption of the nonvolatile memory can be lessened during repeatedly reading/writing operations.

[0006] In order to realize the abovesaid object, a device for prolonging the lifetime of the nonvolatile memory is applied, according to the principles of the invention, to connect a host electronic machine with a nonvolatile memory unit, and comprises a RAM (Random Access Memory) buffer zone, a counter, and two sets of inverters.

[0007] The RAM buffer zone connected to the counter and the inverters is employed for temporary storage of a unit data train and a corresponding state flag during access when a host electronic machine is to read/write from or to the nonvolatile memory, such that the state flag will indicate the operation state when the unit data train passes through the inverters.

[0008] The counter connected with the host electronic machine and the RAM buffer zone is in charge of counting the total bits of logic "0" in the unit data train and judging if the counted result outnumbers a default proportion. If positive, the state flag corresponding to the unit data train is turned into "0", otherwise, into "1".

[0009] The interpolated inverters are arranged to lessen the times of

reading/writing the nonvolatile memory by checking a corresponding state flag of the unit data train to decide whether a logic inversion of the unit data train is needed or not. By doing so, the device of this invention will write relatively fewer bits of logic "0" for prolonging the lifetime of the nonvolatile memory.

[0010] For more detailed information regarding advantages or features of this invention, at least an example of preferred embodiment will be elucidated below with reference to the annexed drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The related drawings in connection with the detailed description of this invention, which is to be made later, are described briefly as follows, in which:

[0012] Fig. 1 shows a hardware framework of a conventional nonvolatile memory device; and

[0013] Fig. 2 shows a hardware framework of a nonvolatile memory device of this invention.

DETAILED DESCRIPTION OF THE INVENTION

[0014] In a hardware framework of a conventional nonvolatile memory device shown in Fig. 1, when an electronic machine 10 is to write a unit data train to a flash memory 130, the unit data train is transmitted from a host electronic machine 110 to the flash memory 130 via a buffer zone 121 of a Random Access Memory (RAM) in a controller 120. On the other hand, when the electronic machine 10 is to read a unit data train stored in the flash memory 130, the operation is reversed. The

afore-mentioned unit data train is substantially a page of data in an average flash memory.

[0015] Fig. 2 shows a hardware framework of a nonvolatile memory device according to a preferred embodiment of the present invention, in which the controller 120 in Fig. 1 is replaced with: a RAM buffer zone 221; a counter 222; and two sets of inverters 223a, 223b.

[0016] The RAM buffer zone 221 is connected to the counter 222 and the inverters 223a, 223b, and is employed for temporary storage of a unit data train and a corresponding state flag during access when a host electronic machine 210 is to read/write from or to a flash memory unit 230, at which time the state flag will indicate the operation state when the unit data train passes through the inverters 223a, 223b. In the illustrated example, the unit data train comprises 528 bytes including 512 bytes for a data district and 16 bytes for recording the state flag corresponding to the unit data train.

[0017] The counter 222 which is connected with the RAM buffer zone 221 is in charge of counting the total bits of logic "0" in the unit data train temporarily stored in the RAM buffer zone 221 and judging if the counted result outnumbers a default proportion, 50% for example. If positive, the state flag corresponding to the unit data train is turned into "0", otherwise, into "1".

[0018] The inverter 223a is arranged to invert the logic phase of the unit data train before the host electronic machine 210 writes the unit data train to the flash memory 230 when the state flag is found to be "0". On the other hand, no logic phase inversion is made in the case the state flag is found to be "1".

[0019] When the host electronic machine **210** is to read a unit data train from the flash memory unit **230** and finds that the state flag is "0", it means that the unit data train to be read has been inverted before. At this time, the data train must be inverted by the inverter **223b** once more for restoration before being read. Contrarily, if the state flag reads "1", the unit data train is ready for the original data to be read without needing any logic inversion. The elaboration of the interpolated inverters **223a, 223b** is in short intended to write fewer bits of logic "0" and thereby prolong the lifetime of the nonvolatile memory.

[0020] In the above described, at least one preferred embodiment has been described in detail with reference to the drawings annexed, and it is apparent that numerous variations or modifications may be made without departing from the true spirit and scope thereof, as set forth in the claims below.